

Dr. Spyros Tragoudas, Ph.D.
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CAD for VLSI and Architectures

This presentation reviews some recent results in testing using the path delay fault model. The huge number of faults requires algorithms and data structures that handle the faults implicitly. Techniques for implicit fault simulation, test pattern generation and cause effect diagnosis will be presented.

Thursday, September 20th
1:00 p.m. to 3:00 p.m.
Engineering Building
Room 1010

Dr. Tragoudas is a Professor in the Department of Electrical and Computer Engineering at Southern Illinois University Carbondale. His research interests are in the areas of Design and Test Automation of Electronic Digital Circuits and in Computer Networks. He has published more than 60 articles in the most prestigious journals in the above areas.

In addition, he has published over 110 papers in the Proceedings of refereed Conferences. He has received three "best paper" awards in prestigious International Conferences in the field of Electronic Design Automation. His publications have been cited in more than 150 journal articles, and even textbooks as is documented in the Science Citation Index. He serves on the Editorial board of one journal and on the program committee of five Conferences in Electronic Design and Test Automation.

Dr. Tragoudas has received more than \$600K in grants from NSF and industry. He was continuously funded from NSF for ten years (1994 -2003). He has also received over \$600K in hardware equipment, and over \$2M in software from industry.

Refreshments will be available.